A

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,104	12/20/2000	Ryo Inoue	10559-391001/P10256-ADI	6933

20985 7590 11/10/2005

FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,104	INOUE ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/19/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7-17 and 19-30* is/are rejected.

7)☒ Claim(s) *2,5,6 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 7-17, and 20-25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Byrne, US Patent 5,537,606 (herein referred to as Byrne).

3. Referring to claim 1 Byrne has taught a method comprising:

a. fetching, by a first pipeline of a pipelined processor, loop conditions corresponding to a particular instance of a loop setup instruction for a first hardware loop (Figure 5B, element 502, r6);

b. first propagating a first of said loop conditions of said first hardware loop via said first pipeline of a pipelined processor (Figure 5B, element 502, r6);

c. piping a second of said loop conditions from said first pipeline of the pipelined processor to a second pipeline of the pipelined processor (Figure 5B, element 502, r6');

d. second propagating in parallel with said first propagating the second of said loop conditions for said first hardware loop corresponding to the particular instance of a loop setup instruction via said second pipeline of the pipelined processor (Figure 5B, element 502, r6 and r6', Figure 1, column 3, lines 45-50, column 4, lines 35-45, column 5, lines 54-63, column 6, lines 47-50, column 9 and 10, column 11, line 45-column 12, line 27).

4. Referring to claim 4, Byrne has taught the method of claim 1, as described above, and further comprising propagating a third of said loop conditions via a third pipeline (Figure 5b, element 501, r0).

5. Referring to claim 7, Byrne has taught a method comprising:

a. first calculating a first loop condition of a first hardware loop from a particular instance of a loop setup instruction using a first arithmetic logic unit in a first pipeline (Figure 5B, element 502, r6, Figure 6 and 7, column 12, line61-column 14, line 26); and

b. second calculating a second loop condition of said first hardware loop from the loop setup instruction using a second arithmetic logic unit in a second pipeline (Figure 5B, element 502, r6', Figure 6 and 7, column 12, line61-column 14, line 26);

c. using results of said first calculating and said second calculating for propagating said loop conditions in each of the first and second pipelines to hardware registers associated with calculating parameters of said first hardware loop (Figure 2, elements 201 and 220, Figure 3, elements 301 and 320); and

d. beginning to calculate said parameters using said first hardware loop, based on said loop conditions, prior to said propagating of said loop conditions in each of the first and second pipelines to the hardware registers (column 11, line 45-column 13, line 21, The loop setup values for r6 and r6', vector offsets, are calculated before they are stored in the registers, see Figure 7.).

6. Referring to claim 8, Byrne has taught the method of claim 7, as described above, and further comprising writing the first and second loop conditions to a first set of registers (column

11, line 45-column 13, line 21, Loop condition values are written into r6 and r6' through the first set of registers, elements 201 and 301.).

7. Referring to claim 9, Byrne has taught the method of claim 7, as described above, and further comprising:

a. calculating a third loop condition of the hardware loop from the particular instance of the loop setup instruction using a third arithmetic logic unit in a third pipeline (Figure 5b, r0); and

b. writing the first, second and third loop conditions to a first set of registers (column 12, lines 5-9, and 11-18).

8. Referring to claim 10, Byrne has taught the method of claim 7, as described above, and wherein calculating the first loop condition and calculating the second loop condition occur in parallel (Figure 5B, element 502, r6 and r6', Figure 1, column 3, lines 45-50, column 4, lines 35-45, column 5, lines 54-63, column 6, lines 47-50, column 9 and 10, column 11, line 45-column 12, line 27).

9. Referring to claim 11, Byrne has taught the method of claim 8, as described above, and further comprising propagating the first loop condition to a second set of registers via a first pipeline (Figures 2 and 3, elements 220 and 320).

10. Referring to claim 12, Byrne has taught the method of claim 11, as described above, and further comprising propagating the second loop condition to the second set of registers via a second pipeline (Figures 2 and 3, elements 220 and 320).

11. Referring to claim 13, Byrne has taught an apparatus comprising:

a. a first pipeline including a first arithmetic logic unit and a second pipeline including a second arithmetic logic unit (Figures 1, 2, and 3, elements 21, 22, 31, and 32), and

b. a control unit coupled to the pipelines (Figure 1, element 2, Figure 2 and 3, I-fetch), the control unit adapted to:

c. obtain loop setup instructions for a first hardware loop from a computer program, the loop setup instructions associated with a particular instance of execution of the first hardware loop (Figure 5b, elements 501-504, column 9, line 31-column 13, line 30);

d. pipe a loop setup instruction from the first pipeline to the second arithmetic unit in the second pipeline (column 9, line 31-column 13, line 30, Figure 5b, element 502 is piped to both pipelines.);

e. first calculate a first loop condition of said particular instance of execution of the first hardware loop from one of said loop setup instructions using the first arithmetic logic unit in the first pipeline (Figure 5B, element 502, r6, Figure 6 and 7, column 12, line61-column 14, line 26);

f. second calculate a second loop condition of said particular instance of execution of the first hardware loop from the piped loop setup instruction using the second arithmetic logic unit in the second pipeline, in parallel with said first calculate (Figure 5B, element 502, r6', Figure 6 and 7, column 12, line61-column 14, line 26).

12. Referring to claim 14, Byrne has taught the apparatus of claim 13, as described above, and further comprising a first set of registers coupled to the control unit, wherein the control unit

is further adapted to write the first and second loop conditions of the hardware loop to the first set of registers (Figures 1-3, elements 201, 218, 301, and 316).

13. Referring to claim 15, Byrne has taught the apparatus of claim 14, as described above, and further comprising a third pipeline coupled to the control unit, the third pipeline including a third arithmetic logic unit, the control unit further adapted to:

a. calculate a third loop condition of the hardware loop from the loop setup instruction using the third arithmetic logic unit in the third pipeline (r0 LVL, Figure 5a, element 501); and

b. write the first, second and third loop conditions of the particular instance of execution of the hardware loop to the first set of registers (column 11, line 45-column 13, line 21, Loop condition values are written into r6, r6', and r0 through the first set of registers, elements 201 and 301.).

14. Referring to claim 16, Byrne has taught the apparatus of claim 14, and further comprising a second set of registers coupled to the control unit, wherein the control unit is further adapted to propagate at least one of the loop conditions to the second set of registers via the first pipeline (Figures 2 and 3, elements 220 and 320).

15. Referring to claim 17, Byrne has taught the apparatus of claim 16, and further adapted to propagate at least one of the loop conditions to the second set of registers via the second pipeline (Figures 2 and 3, elements 220 and 320).

16. Referring to claim 20, Byrne has taught the apparatus of claim 13, as described above, and wherein at least one of the pipelines is a data address generation pipeline (column 8, lines 10-21).

17. Referring to claim 21, Byrne has taught the apparatus of claim 13, as described above, and wherein at least one of the pipelines is a system pipeline (Figures 1-3, all pipelines are system pipelines).

18. Referring to claim 22, Byrne has taught an apparatus comprising a set of registers (Figures 2 and 3, elements 220, 320, 201, 218, 301, and 316), a first pipeline (Figures 1-3, elements 21 and 31), and a second pipeline (Figures 1-3, elements 22 and 32 for vector extensions); and

a. a control unit coupled to the set of registers, the first pipeline and the second pipeline (Figure 1, element 2), the control unit adapted to:

b. first propagate at least one loop condition of a particular instance of execution of a first hardware loop to the set of registers via the first pipeline (Figure 5b, elements 501-504, r0, r6, r7, r8. Figures 1-3);

c. second propagate at least one loop condition of the particular instance of execution of said first hardware loop to the set of registers via the second pipeline (Figures 1-3, Vector extension pipelines propagate loop conditions.); and

d. begin calculating data using said first hardware loop, prior to propagating the at least one loop condition of a particular instance of execution of said first hardware loop in the first pipeline to the set of registers and prior to propagating the at least one loop condition of the particular instance of execution of said first hardware loop in the second pipeline to the set of registers (Figure 5b, element 501, Figure 1, element 3).

19. Referring to claim 23, Byrne has taught the apparatus of claim 22, as described above, and wherein the set of registers are a second set of registers, the apparatus further including a

first set of registers coupled to the control unit (Figures 2 and 3, elements 301, 316, 201, and 218), wherein the control unit is further adapted to:

a. write the loop conditions of the particular instance of execution of the hardware loop to the first set of registers prior to propagating at least one of the loop conditions to the second set of registers (Figures 2 and 3).

20. Referring to claim 24, Byrne has taught the apparatus of claim 22, as described above, and wherein at least one of the pipelines is a data address generation pipeline (column 8, lines 10-21).

21. Referring to claim 25, Byrne has taught the apparatus of claim 22, as described above, and wherein at least one of the pipelines is a system pipeline (Figures 1-3, all pipelines are system pipelines).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne, in view of Tran U.S. Patent Number 6,003,128 (herein referred to as Tran).

24. Referring to claim 19 Byrne has not taught wherein the first set of registers are speculative registers. Tran has taught a first set of registers are speculative registers (Tran abstract). Tran has taught that using speculative processing with predictions reduces the processing time needed by the system to complete a program (Tran column 2 line 34-column 3

line 5). One of ordinary skill in the art at the time of the invention would have recognized that adding speculative loop prediction and execution to Byrne would increase the speed of the loop execution taking place in the system of Byrne. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement speculative loop processing to increase the speed of execution of the instructions.

25. Claims 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne.

26. Referring to claim 26 Byrne has taught a system comprising:

a. wherein a processor includes a first set of registers (Figures 2 and 3, elements 201, 218, 301, and 316), a first pipeline (Figures 2 and 3, elements 21 and 31), a second pipeline (Figures 2 and 3, elements 22 and 32), and a control unit (Figure 1, element 2) adapted to:

i. pipe a loop setup instruction from the first pipeline to a second arithmetic unit in the second pipeline (vector extensions, Figures 1-3, elements 22 and 32, Figure 5b, r6, r7, r8, and elements 501-504);

ii. first calculate a first loop condition of a particular instance of execution of a first hardware loop from the loop setup instruction using a first arithmetic logic unit in the first pipeline (Figure 5B, element 502, r6, Figure 6 and 7, column 12, line61-column 14, line 26);

iii. second calculate a second loop condition of said particular instance of execution of the first hardware loop from the loop setup instruction using the second arithmetic logic unit in the second pipeline, in parallel with the first

calculate (Figure 5B, element 502, r6', Figure 6 and 7, column 12, line61-column 14, line 26).

27. Byrne has not taught a static random access memory device and a processor coupled to the static random access memory device. Byrne has taught a cache and a processor coupled to the cache (Byrne, Figure 1). Official Notice is taken that it is well known in the art that caches are implemented using static random access memory. One of ordinary skill in the art at the time of the rejection would recognize that using static random access memory would allow the cache memory to provide the instructions and data to the processor faster that dynamic random access memory, thus making static random access memory a more desirable memory for caches. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use static random access memory as the cache memory of Byrne to provide the instructions and data more quickly to the processor, which reduces the time required by execution.

28. Claim 27 is rejected for the same reasons as described in the rejection to claim 9.

29. Referring to claim 28, Byrne has taught a system comprising:

a. wherein the processor includes a first set of registers (Figures 2 and 3, elements 220, 320, 201, 218, 301, and 316), a second set of registers (Figures 2 and 3, elements 220 and 320), a first pipeline (Figures 1-3, elements 21 and 31), a second pipeline (Figures 1-3, elements 22 and 32 for vector extensions), and a control unit (Figure 1, element 2) adapted to:

b. write loop conditions of a first hardware loop to the first set of registers (Figure 5b, elements 501-504, Figures 1-3, elements 201, 218, 301, and 316);

c. propagate at least one of the loop conditions of said first hardware loop to the second set of registers via the first pipeline (Figures 2 and 3, elements 220 and 320); and

d. propagate at least one of the loop conditions of said first hardware loop to the second set of registers via the second pipeline (vector extension pipelines, elements 22 and 32, elements 220 and 320); and

e. begin calculating data using said first hardware loop prior to propagation of the at least one of the loop conditions of said first hardware loop in the first pipeline to the second set of registers and prior to propagation of the at least one of the loop conditions of said first hardware loop in the second pipeline to the second set of registers (Figure 5b, element 501, Figure 1, element 3).

30. Byrne has not taught a static random access memory device and a processor coupled to the static random access memory device. Byrne has taught a cache and a processor coupled to the cache (Byrne figure 1). Official Notice is taken that it is well known in the art that caches are implemented using static random access memory. One of ordinary skill in the art at the time of the rejection would recognize that using static random access memory would allow the cache memory to provide the instructions and data to the processor faster that dynamic random access memory, thus making static random access memory a more desirable memory for caches. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use static random access memory as the cache memory of Byrne to provide the instructions and data more quickly to the processor, which reduces the time required by execution.

31. Referring to claim 29, Byrne has taught the system of claim 29, as described above, and further including a third pipeline, the control unit further adapted to propagate at least one of the loop conditions to the second set of registers via the third pipeline (Figures 1-3).

32. Referring to claim 30, Byrne has taught the system of claim 28, as described above, and further adapted to:

a. calculate a first loop condition of the hardware loop from a loop setup instruction using a first arithmetic logic unit in the first pipeline (Figure 5B, element 502, r6, Figure 6 and 7, column 12, line61-column 14, line 26); and

b. calculate a second loop condition of the hardware loop from the loop setup instruction using a second arithmetic logic unit in the second pipeline (Figure 5B, element 502, r6', Figure 6 and 7, column 12, line61-column 14, line 26).

Response to Arguments

33. Applicant's arguments with respect to claims 1, 4, 7-17, 19-30 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

34. Claims 2, 5, 6, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

10/28/05

HENRY W. H. TSAI
PRIMARY EXAMINER